

USPS EXPRESS MAIL
EV 338 198 822 US
FEBRUARY 04 2004

Description

Technical field

[0001] The present invention relates to an information communication device, such as a non-contact tag or non-contact IC card, that processes a signal by obtaining electric power from an electric wave transmitted from an antenna.

Background art

[0002] Conventionally, non-contact tags have been in use that transmit the information stored in themselves by acquiring electric power from an electric wave transmitted from somewhere else. Non-contact tags are used, for example, with the lift facilities at a skiing ground, with the ticket examination equipment at a railway station, and for sorting of baggage.

[0003] Such a non-contact tag has a transmitter/receiver unit incorporated therein, but not a power source such as a battery. A non-contact tag obtains electric power from an electric wave (a high-frequency signal) it receives. Thus, a non-contact tag, despite incorporating no battery, permits exchange of information for a long period of time. Moreover, a non-contact tag achieves exchange of information by an electric wave or by magnetic induction, and thus offers the advantage of exchanging information on a non-contact basis.

[0004] On the other hand, for the purpose of recording or, inversely, offering information, IC cards are already in practical use that permit exchange of information with a reader/writer on a non-contact basis (thus by an electric wave or by magnetic induction). Such an IC card, too, obtains electric power from an electric wave it receives or through magnetic induction.

[0005] In Fig. 9, reference numeral 90 represents a reader/writer, with only a transmission antenna (coil L_s) provided therein shown as a constituent component thereof. On the other hand, reference numeral 91 represents an IC card, reference numeral 92 represents a tuning circuit thereof, and reference numerals 93 and 94 represent a rectifying diode and a smoothing capacitor, respectively. The tuning circuit 92 is composed of a reception antenna (coil L_p) and a tuning capacitor C_0 . An electric wave transmitted from the reader/writer 90 is received by the tuning circuit. The thus received high-frequency signal is rectified by the rectifying diode 93 and is then smoothed by the smoothing capacitor 94 so as to be used as a power source by the IC card 91.

[0006] The intensity (amplitude level) of the high-frequency signal received by and output from the tuning circuit 92 varies according to the distance between the reader/writer 90 and the IC card 91; specifically, the shorter the distance, the more intense the signal, and, the longer the distance, the less intense the signal. Thus, the reproduction efficiency with which electric

power is produced by rectifying the received high-frequency signal also varies according to the distance between the reader/writer 90 and the IC card 91.

[0007] As a result, quite inconveniently, the range of electric power that needs to be fed to the IC card to ensure its normal operation (in other words, the range of non-contact distance) is rather limited (narrow). Such a limited range of acceptable input voltages makes the IC card unusable in applications in which the input voltage tends to vary greatly. For this reason, it is customary to limit the specifications of IC cards in accordance with their applications (i.e. manufacture separate models for short-distance and long-distance applications). This, however, requires extra cost and causes inconvenience. [0008] Moreover, in this conventional example, a diode is used as a rectifying means, and this diode cannot be used simultaneously as a tuning capacitor. Thus, it is inevitable to provide a capacitor separately in the tuning circuit or secure a capacitance by making the tuning coil larger.

Disclosure of the invention

[0009] An object of the present invention is to provide a communication device that accepts a larger range of input voltages.

[0010] Another object of the present invention is to provide a communication device in which a rectifying means is used to secure a capacitance for a tuning circuit.

[0011] To achieve the above objects, according to the present invention, in a communication device that produces electric power by rectifying a received high-frequency signal, a MOS transistor is connected to an antenna so that the received signal is rectified by a parasitic diode of the MOS transistor. In this case, the capacitance accompanying the MOS transistor influences the input tuning frequency.

[0012] The communication device may be provided with, as the above-mentioned MOS transistor, one or more MOS transistors, and in addition have control means for controlling the on/off states of the transistors. This control means controls the MOS transistors in such a way as to change the tuning frequency in the direction in which the rectified output becomes equal to a predetermined level. The communication device is built, for example, as an IC card that receives the signal from a reader/writer on a non-contact basis.

[0013] Thus, according to the present invention, a communication device produces electric power by rectifying a received high-frequency signal. The received signal is rectified by a parasitic diode of a MOS transistor that is connected to an antenna. The capacitance accompanying the MOS transistor serves as an input tuning capacitance. Switching the on/off state of the transistor causes the capacitance added to that of an input tuning capacitor to change; accordingly, the input tuning frequency changes and the relation between the

input tuning frequency and the frequency of the received high-frequency signal changes. As a result, the amplitude of the received high-frequency signal changes and thus the obtained power also changes.

Brief description of drawings

[0014]

Fig. 1 shows a circuit diagram of a principal portion of the information communication device of a first embodiment of the present invention. Fig. 2 shows circuit diagrams illustrating the input tuning circuit thereof. Fig. 3 shows circuit diagrams illustrating how the frequency of the input tuning circuit is changed. Fig. 4 shows a diagram illustrating how the selectivity of the tuning circuit changes according as the tuning frequency thereof is changed. Fig. 5 shows diagrams illustrating the MOS transistor used in the present invention. Fig. 6 shows a circuit diagram of a principal portion of the information communication device of a second embodiment of the present invention. Fig. 7 shows an equivalent circuit diagram illustrating how rectification is achieved therein. Fig. 8 shows diagrams illustrating how the present invention is used in practice. Fig. 9 shows a circuit diagram of a principal portion of a conventional information communication device.

Best mode for carrying out the invention

[0015] Hereinafter, embodiments of the present invention will be described with reference to the accompanying drawings. In Fig. 1, reference numeral 1 represents a reader/writer, and reference numeral 2 represents a signal source thereof. Reference numerals 3 and 4 represent a capacitor and an inductance coil, which together constitute a tuning circuit of the reader/writer. The inductance coil 4 serves as an antenna.

[0016] Reference numeral 5 represents an IC card. Reference numeral 6 represents a tuning circuit thereof, which is composed of an inductance coil L and a capacitor C_0 . The inductance coil L serves as an antenna. Reference symbol C_A represents a smoothing capacitor connected to one end of the tuning circuit 6, and reference numeral 7 represents a regulator for regulating the output voltage thereof. The output of the regulator 7 is fed to a signal processing circuit (not shown) or the like.

[0017] Reference symbols T_1 and T_2 represent a first and a second MOS transistor, respectively, which are both of an N-channel type, have their drains connected to the other end of the tuning circuit 6 (i.e. to the other end of the antenna L), have their sources left open (non-connected), and have their gates connected to a control circuit 9. Reference numeral 8 represents a detector for detecting the output voltage (or output current) of the smoothing capacitor C_A , and its detection

output is fed to the control circuit. The control circuit 9 controls the on/off state of the transistors T_1 and T_2 in accordance with the detection output.

[0018] Reference symbols D_1 and D_2 represent parasitic diodes that accompany the MOS transistors T_1 and T_2 . These diodes serve as rectifying diodes. Reference symbols C_1 and C_3 represent the drain junction capacitances of the transistors T_1 and T_2 , and reference symbols C_2 and C_4 represent the source junction capacitances thereof. In Fig. 5, at (a) is shown the schematic symbol of an N-channel MOS transistor, and at (b) is shown the structure thereof together with the junction capacitances C_1 and C_2 and the parasitic diode D_1 mentioned above. In addition to these junction capacitances, another capacitance also exists between the gate and drain in reality; however, for simplicity's sake, this capacitance is omitted here.

[0019] Now, let the capacitance accompanying the above-mentioned MOS transistors be C_B , then the capacitors arranged in an input-side portion of the IC card 5 have a relationship as shown at (a) in Fig. 2. Here, if it is assumed that C_A is much greater than C_B (i.e. $C_A \gg C_B$), then the circuit shown at (a) in Fig. 2 is equivalent to the circuit shown at (b) in Fig. 2. Thus, the tuning frequency f of the tuning circuit is given as

$$f=1/[2\pi\{L(C_0+C_B)\}^{1/2}]$$

[0020] When the transistors T_1 and T_2 are both off, the source-side capacitances C_2 and C_4 thereof do not function. Accordingly, as shown at (a) in Fig. 3, $C_B=C_1+C_3$, and thus the tuning frequency f_1 is given as

$$f_1=1/[2\pi\{L(C_0+C_1+C_3)\}^{1/2}]$$

[0021] When the transistors T_1 and T_2 are both on, the source-side capacitances C_2 and C_4 thereof function. Accordingly, as shown at (b) in Fig. 3, $C_B=C_1+C_2+C_3+C_4$, and thus the tuning frequency f_2 is given as

$$f_2=1/[2\pi\{L(C_0+C_1+C_2+C_3+C_4)\}^{1/2}]$$

[0022] When the transistor T_1 is on and the transistor T_2 is off, as shown at (c) in Fig. 3, $C_B=C_1+C_2+C_3$, and thus the tuning frequency f_3 is given as

$$f_3=1/[2\pi\{L(C_0+C_1+C_2+C_3)\}^{1/2}]$$

[0023] When the transistor T_1 is off and the transistor T_2 is on, simply C_4 is substituted for C_2 in the above equation, and $C_2=C_4$ from the beginning. Accordingly, also in this case, the tuning frequency equals f_3 .

[0024] The tuning frequencies given above have a relation $f_2 < f_3 < f_1$, and this can be illustrated in terms of selectivity Q of the tuning circuit as shown in Fig. 4. Now, suppose that the distance between the

reader/writer 1 and the IC card 5 is constant and that the frequency of the high-frequency signal transmitted from the reader/writer 1 equals f_1 . Under these conditions, when the tuning frequency of the IC card 5 equals f_1 , the received signal has the largest amplitude, and thus the largest amount of electric power is obtained; when the tuning frequency equals f_2 , the smallest amount of electric power is obtained; when the tuning frequency equals f_3 , a medium amount of electric power is obtained. Usually, as long as the tuning frequency is kept constant, the longer the distance between the reader/writer 1 and the IC card 5, the smaller the amount of the obtained electric power.

[0025] On the basis of the output voltage (or current) of the smoothing capacitor C_A as detected by the detector 8, the control circuit 9 controls the on/off state of the transistors T_1 and T_2 . For example, the transistors T_1 and T_2 are controlled in accordance with whether the detected value is greater or less than a previously determined reference value.

[0026] In this embodiment, for example when the reader/writer 1 and the IC card 5 are too distant from each other to obtain a sufficient amount of electric power, the tuning frequency of the IC card 5 is set to be equal to f_1 , at which tuning is achieved perfectly. By contrast when the reader/writer 1 and the IC card 5 are so close to each other that an excessive amount of electric power is obtained, the tuning frequency of the IC card 5 is set to be equal to f_2 or f_3 , at which tuning is achieved imperfectly.

[0027] Here, it is to be noted that the control circuit 9 controls the on/off state of the transistors T_1 and T_2 solely in accordance with whether the detected voltage (or current) is higher or lower than the reference value and thus irrespective of the distance between the reader/writer 1 and the IC card. Therefore, if a sufficient amount of electric power cannot be obtained even though the reader/writer 1 and the IC card 5 are sufficiently close to each other, the tuning frequency is changed.

[0028] The embodiment described above deals with a case where half wave rectification is used. However, the present invention can be applied also to cases where full-wave rectification is used. Fig. 6 shows an embodiment for such cases. In Fig. 6, an inductance coil L and a capacitor C_0 together constitute a tuning circuit 6, which is, at both ends, connected to a group of MOS transistors.

[0029] Reference symbols Q1 to Q6 represent n-channel MOS transistors, and reference symbols Q7 to Q12 represent p-channel MOS transistors. The transistors Q1 to Q3 have their drains connected to one end α of the tuning circuit 6, and have their substrates connected to ground. The transistors Q4 to Q6 have their drains connected to the other end β of the tuning circuit 6, and have their substrates connected to ground. The transistors Q1 to Q6 have their gates connected to a control register 81.

[0030] On the other hand, the transistors Q7 to Q9 have their drains connected to one end α of the tuning circuit 6, and have their substrates connected to an output path 83. The transistors Q10 to Q12 have their drains connected to the other end β of the tuning circuit 6, and have their substrates connected to the output path 83. The transistors Q7 to Q12 have their gates connected to a control register 82. The transistors Q1 to Q12 all have their sources left open.

[0031] How parasitic diodes and capacitances appear in the n-channel MOS transistors Q1 to Q6 is indicated, using the transistor Q6 as their representative, by reference numerals 84, 85, and 86. Reference numeral 84 represents a parasitic diode that appears between the drain and substrate of the transistor Q6, reference numeral 85 represents a junction capacitance appearing at the same location, and reference numeral 86 represents a source-side junction capacitance.

[0032] On the other hand, how parasitic diodes and capacitances appear in the p-channel MOS transistors Q7 to Q12 is indicated, using the transistor Q12 as their representative, by reference numerals 87, 88, and 89. Reference numeral 87 represents a parasitic diode that appears between the drain and substrate of the transistor Q12, reference numeral 88 represents a junction capacitance appearing at the same location, and reference numeral 89 represents a source-side junction capacitance.

[0033] Fig. 7 is an equivalent circuit diagram of the full-wave rectification circuit shown in Fig. 6. A rectifying diode 11 and a capacitor 21 are formed by the transistors Q7 to Q9, and a rectifying diode 12 and a capacitor 22 are formed by the transistors Q10 to Q12. Similarly, a rectifying diode 13 and a capacitor 23 are formed by the transistors Q4 to Q6, and a rectifying diode 14 and a capacitor 24 are formed by the transistors Q1 to Q3. Here, the capacitances of the capacitors 21, 22, 23, and 24 change in accordance with whether the corresponding transistors are on or off.

[0034] In accordance with whether the voltage (or current) at the output path 83 is higher or lower than a predetermined value, a detection circuit 80 controls the control transistors 81 and 82 and thereby controls the on/off state of the transistors Q1 to Q12.

[0035] In the circuit shown in Fig. 6, where full-wave rectification is used, no smoothing capacitor like C_A shown in Fig. 1 is provided; however, it is of course possible to provide one if required. In both of the embodiments shown in Figs. 1 and 6, an inductance coil L is used in the tuning circuit 6; however, instead of a coil, it is possible to use anything that serves as an inductance, such as a mere conductor piece, pattern, or the like. The tuning capacitor C_0 does not need to be provided separately; instead, it is possible to use the distributed capacitance of the coil L , or to rely totally on the capacitances of the transistors T_1 and T_2 or Q1 to Q12.

[0036] In Fig. 8, at (a) is shown a case where the IC card 5 has separate input tuning circuits 101 and 102,

one for electric power reproduction and one for signal transfer, and at (b) is shown a case where the IC card 5 uses a single input tuning circuit 101 for both purposes. In the case shown at (a), the transmitter side transmits a continuous wave having a frequency f_H for electric power reproduction and a signal having a carrier frequency f_L . In this case, even if the tuning frequency of the input tuning circuit 101 for electric power adjustment is changed by changing the capacitance of the rectification circuit 103, the tuning frequency of the input tuning circuit 102 for signal transfer is not affected.

[0037] In the case shown at (b), on a single carrier having an identical frequency, a signal period t_1 for reproduction of electric power and a signal period t_2 for transfer of a signal proper are time-shared. In this case, the changing of the input tuning frequency as achieved by the changing of the capacitance of the rectification circuit 103 may be inhibited. However, where insufficiency of the input electric power is correlated with an excessively low level of the signal proper, it is preferable to let the rectification circuit 103 continue the changing of the input tuning frequency even during the signal period.

Industrial applicability

[0038] As described above, according to the present invention, a single device, namely a MOS transistor, can be used simultaneously as a rectifying diode and as a tuning capacitor. In addition, the capacitance (and thus the tuning frequency) can be changed easily by turning on and off the transistor. Moreover, a plurality of MOS transistors can be formed easily in a compact IC. Furthermore, considering that an information communication device incorporates digital circuits for signal processing and that such digital circuits are often formed by the use of MOS transistors, it is preferable, from the viewpoint of designing, manufacture, and costs, to form also rectifying diodes and tuning capacitors by the use of MOS transistors as in the present invention. Offering these advantages, the present invention can be suitably applied to a communication device that produces electric power by rectifying a received high-frequency signal, such as an IC card that receives a signal from a reader/writer on a non-contact basis.

Claims

1. A communication device that produces electric power by rectifying a received high-frequency signal, wherein a MOS transistor is connected to an antenna so that the received signal is rectified by a parasitic diode of the MOS transistor.
2. A communication device as claimed in claim 1, wherein a capacitance accompanying the MOS transistor influences an input tuning frequency.

3. A communication device as claimed in claim 2, wherein, as the MOS transistor, one or more MOS transistors are provided, and control means is provided for controlling on/off states of the transistors.
4. A communication device as claimed in claim 3, wherein the control means controls the MOS transistors in such a way as to change a tuning frequency in a direction in which a rectified output becomes equal to a predetermined level.
5. A communication device as claimed in claim 1, wherein the communication device is built as an IC card that receives the signal from a reader/writer on a non-contact basis.

FIG. 1

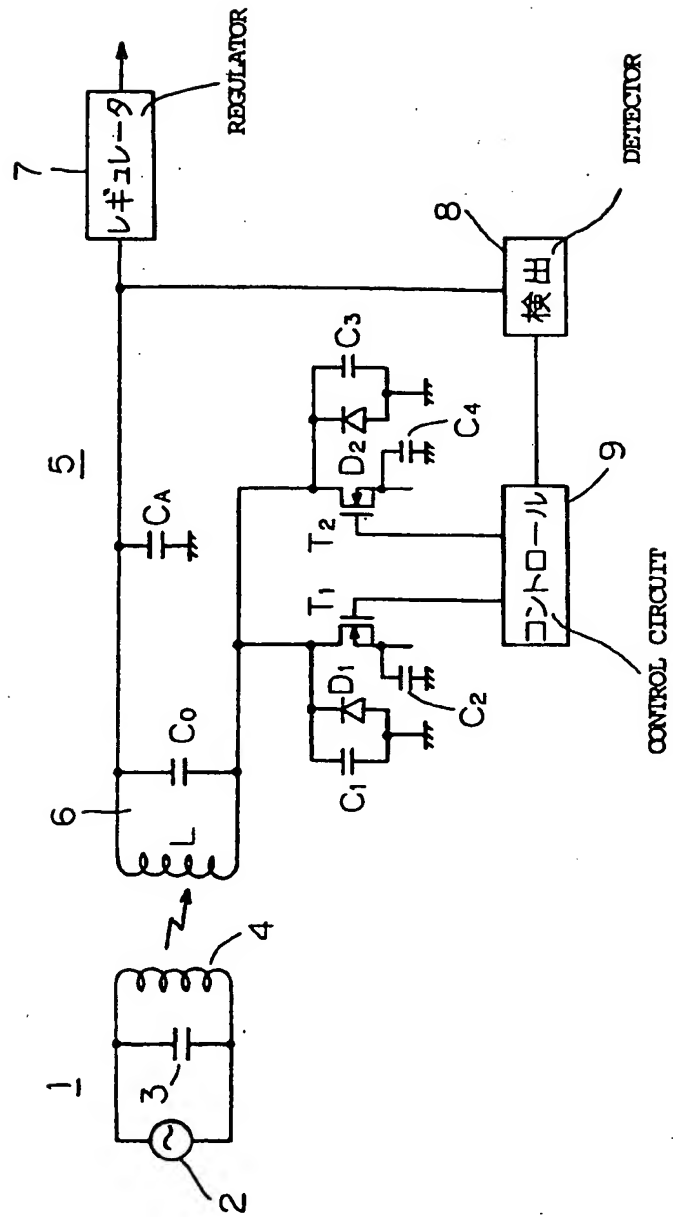


FIG.2

~~FIG. 2~~

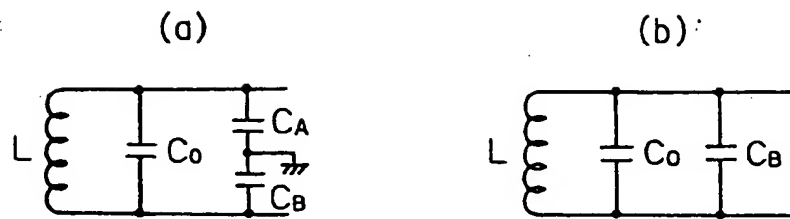


FIG.3

~~FIG. 3~~

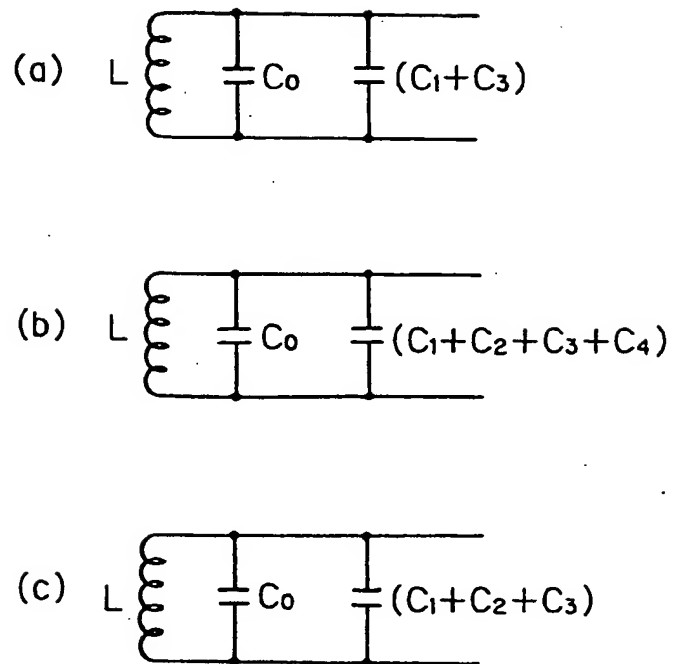


FIG. 4

~~FIG. 4~~

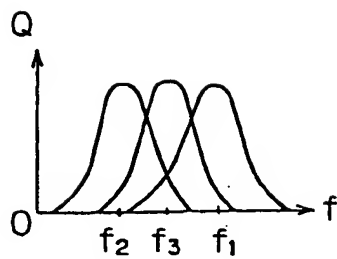
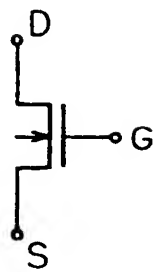
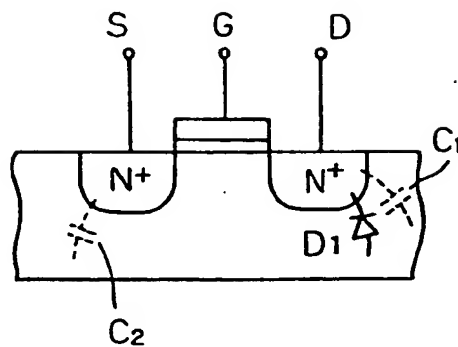


FIG. 5

~~FIG. 5~~



(a)



(b)

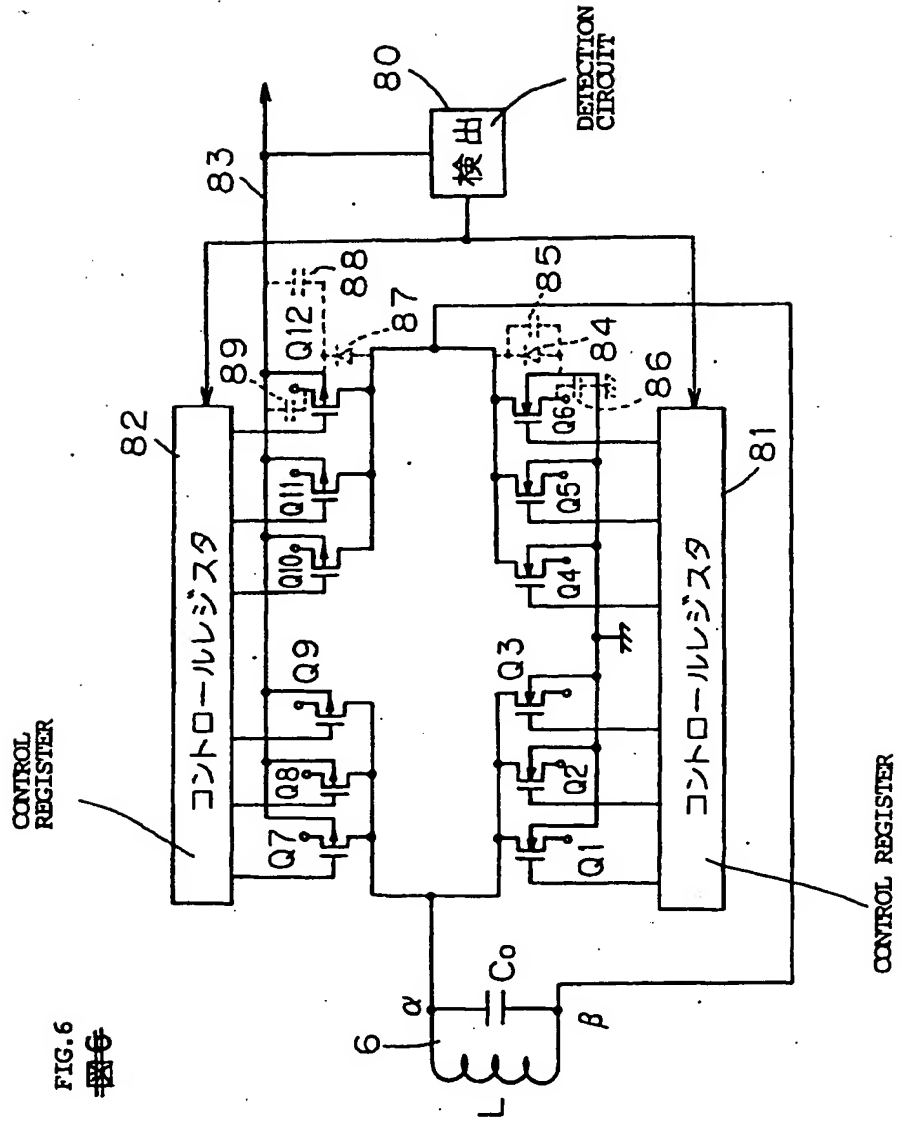


FIG. 7

図7

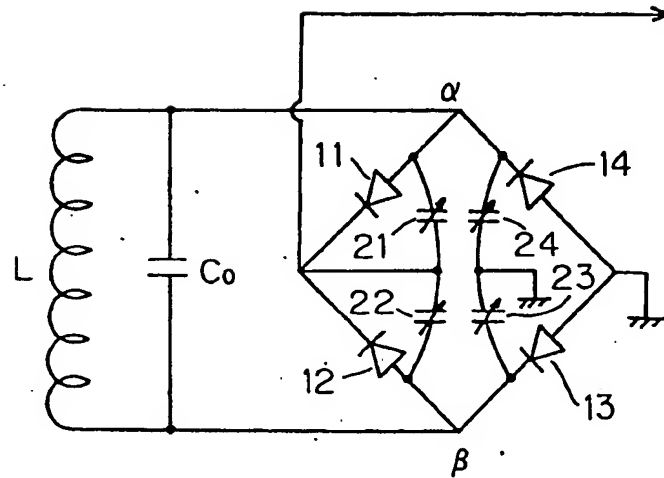


FIG. 8

図8

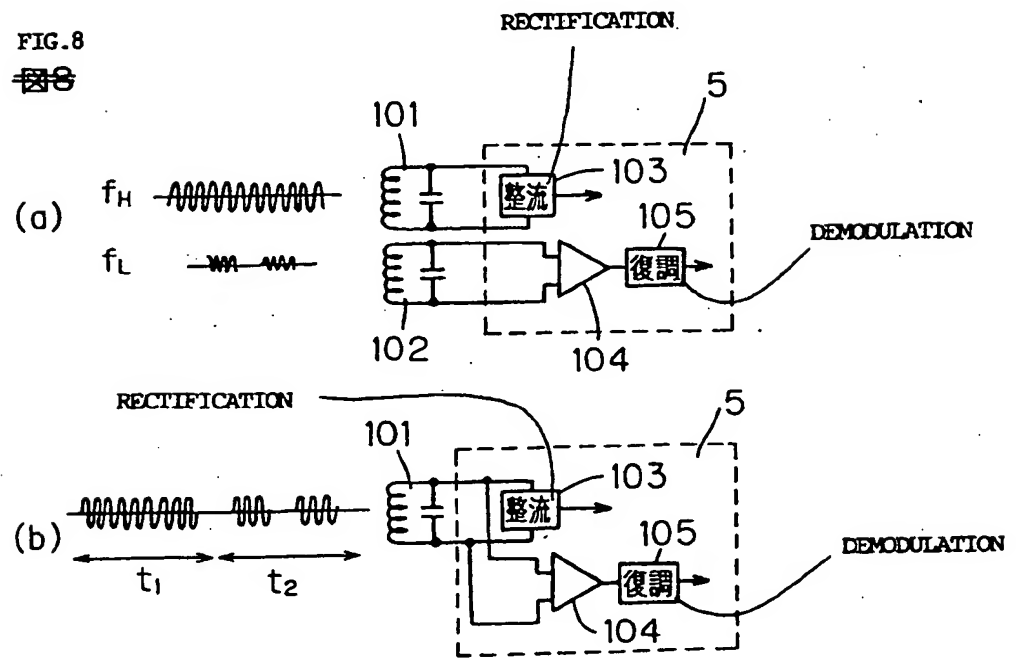
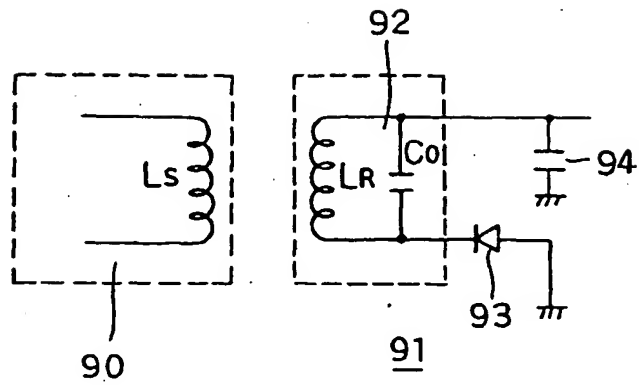


FIG. 9

~~FIG. 9~~



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP98/05138A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl.⁴ H04B1/59, 5/00, G06K19/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl.⁴ H04B1/59, 5/00, G06K19/00Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1997 Toroku Jitsuyo Shinan Koho 1994-1997
Kokai Jitsuyo Shinan Koho 1971-1997 Jitsuyo Shinan Toroku Koho 1996-1997

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP, 8-323657, A (Seiko Epson Corp.),	1
Y	10 December, 1996 (10. 12. 96) (Family: none)	5
A		2-4
Y	JP, 8-185497, A (Sony Corp.),	5
A	16 July, 1996 (16. 07. 96) (Family: none)	1-4
A	JP, 63-190559, A (NEC Corp.),	1-5
	8 August, 1988 (08. 08. 88) (Family: none)	
A	JP, 5-28328, A (Hitachi Maxell, Ltd.),	1-5
	5 February, 1993 (05. 02. 93)	

☐ Further documents are listed in the continuation of Box C.
 ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"B" earlier document but published on or after the international filing date

"L" document which may throw doubt on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"A" document member of the same patent family

Date of the actual completion of the international search
6 February, 1999 (08. 02. 99)Date of mailing of the international search report
23 February, 1999 (23. 02. 99)Name and mailing address of the ISA/
Japanese Patent Office

Authorized officer

Facsimile No.

Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)